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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/944,171
Filing Date: September 04, 2001
Appellant(s): KER ET AL.

MAILED

Joe McKinney Murcy
For Appellant

AUG 02 2006

GROUP 2800

EXAMINER'S ANSWER

This is in response to the appeal brief filed 010406 appealing from the Office action mailed 07/29/03.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

A substantially correct copy of appealed claims 1 – 17 appears on pages A-1 to A-3 of the Appendix to the appellant's brief. The minor errors are as follows: Applicant does not list the other pending claims of the application (18 – 26) with the status modifier "withdrawn."

(8) Evidence Relied Upon

6,406,948 B1	Jun et al.	6-2002
5,623,156	Watt	4-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Rejections - 35 USC § 102

1 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 13, 14, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Jun et al. (U.S. Patent No. 6,406,948 BO).

In re claim 1, Jun discloses an ESD protection circuit with low input capacitance (stacked diodes), suitable for an I/O pad, comprising a plurality of diodes (Fig. 10), stacked and coupled between a first power line (VDD) and the I/O pad (Input), wherein during normal operation, the diodes are reverse-biased, and, when an ESD event occurs between a second power line (Vss) and the I/O pad, the diodes are forward-biased to conduct ESD current.

In re claim 13, Jun (Fig. 9) discloses the device of claim 1, wherein the diode includes a PN junction diode formed by a PN junction between a first source/drain and substrate (P-type) of a MOS.

In re claim 14, Jun discloses the device of claim 13, but does not expressly disclose the gate electrodes connected to power lines. However, one skilled in the art will recognize that gate electrodes being connected to power lines are a necessary condition for any MOS type device to work. That the gate electrodes of Jun, if not specifically mentioned, are connected to power lines is inherent.

In re claims 16 and 17, Jun discloses MOS transistors but does not expressly disclose the conductivity of the transistors. Those skilled in the art will recognize the interchangeability of the two types of devices and will recognize the suitability of

selecting either an NMOS or PMOS configuration to be determined by the suitability of the intended use of the claimed device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun et al. (as above).

In re claim 2, Jun discloses the device of claim 1, wherein each diode is a PN junction diode formed by placing a doped area of a first conductivity type in a first well (16) of a second conductivity type, a deep well (12) of the first conductivity type formed under the first well to isolate the first well from a substrate (10) of the second conductivity type.

Jun does not expressly disclose a doped area a first conductivity type in the first well (16). However, it would have been obvious for one skilled in the art at the time the invention was made to insert such a region for the purpose of increasing the threshold voltage of the ESD device.

In re claim 3, Jun discloses the device of claim 2, wherein the first well (16) is surrounded by a second well (12) of the first conductivity type.

In re claim 4, Jun discloses the device of claim 2, wherein the first conductivity type is N type and the second conductivity type is P type.

Claims 5-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun as

applied to claim 1 above, and further in view of Watt (U.S. Patent No. 5,623,156).

In re claim 5, Jun discloses the device of claim 1, but does not expressly disclose an ESD clamp. Watt discloses an ESD clamp circuit (24). It would have been obvious for one skilled in the art at the time of the invention to use as ESD clamp circuit as disclosed by Watt for the device of Jun for the purpose, for example, of enhancing ESD protection to the internal circuit.

In re claim 6, Jun in view of Watt discloses the device of claim 5, wherein the power-rail ESD clamp circuit includes a substrate triggered MOS including two source/drain (34, 36) coupled to the first power line and the second power line respectively, the substrate node biased with suitable current to trigger a BJT (44), parasitizing in the substrate-triggered MOS, and conducting ESD current when an ESD event occurs.

In re claim 7, Jun in view of Watt discloses the device of claim 6, wherein the substrate-triggered MOS includes a gate applied with a bias voltage. The limitation, "to keep the substrate

"operations" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 8 Jun in view of Watt discloses the device of claim 6, wherein the gate is applied with a bias voltage. The limitation, "to speed up ... occurs" is a recitation of the intended use of the claimed invention and without a more defining structural limitation, is not given patentable weight as to the structure of the device.

In re claim 9, Jun in view of Watt discloses the device of claim 6, but does not expressly disclose the substrate-triggered MOS formed in a first well of a first conductivity type surrounded by a second well of the second conductivity type. However, it would have been obvious for one skilled in the art at the time the invention was made to form the MOS device in wells of this type because it is well known in the art to place transistor devices in doped well for the purpose, for example, of providing better device isolation as compared to simply forming the devices in the substrate, where they may be susceptible to back surface stray currents and voltages.

In re claim 10, Jun in view of Watt discloses the device of claim 9, wherein the first well is surrounded by a second well of the first conductivity type.

In re claim 11, Jun in view of Watt discloses the device of claim 5, wherein the power-rail ESD clamp circuit includes an ESD detection circuit to detect the occurrence of the ESD event.

In re claim 12, Jun discloses the device of claim 1, but does not expressly disclose a MOS diode. Watt discloses a MOS diode (20). It would have been obvious to one skilled in the art at the time the invention was made to utilize an additional diode in the form of a MOS diode as disclosed by Watt for the purpose, for example, of providing secondary ESD protection (Watt; column 8, lines 30-33).

In re claim 15, Jun discloses the device of claim 13, but does not expressly disclose the gate of the MOS couples to a second source/drain of the MOS. Watt discloses the configuration of the gate of a MOS being coupled to the source/drain of a MOS. It would have been obvious to one skilled in the art at the time the invention was made to utilize an additional diode in the form of a MOS diode as disclosed by Watt for the purpose, for example, of providing secondary ESD protection (Watt; column 8, lines 30-33).

(10) Response to Argument

Applicant's arguments have been fully considered but they are not persuasive.

Rejection of Claim 1 as being anticipated by Jun et al. (U.S. Patent No. 6,406,948).

On pp. 5 of the Appeal Brief, applicant questions whether the Jun et al. reference means to show stacked diodes in Fig. 10. Applicant admits that Fig. 10 as disclosed by Jun et al. "could be a basis for this rejection," but submits that the description of the remaining figures is contradictory to the possibility of having stacked diodes in Fig. 10. Applicants suggest that the Patentee has used an incorrect symbol to indicate large area diodes and that Fig. 10 only appears to describe the claimed stacked diode structure.

Applicant cites MPEP 716.07 to show that an error in a prior art disclosure is not put in the possession of the public. However, the language applicant cites refers to a typographical error admitted to by a co-author of a literature article, not a patentee. However, even if the patentee had filed an affidavit or declaration that he or she did not intend the disclosed invention to be used as claimed by applicant is immaterial, if the patent teaches or suggests the claimed invention. *In re Pio*, 217 F.2d 956, 104 USPQ 177 (CCPA 1954). In this case, there is no such disclaimer by the patentee. Rather, Fig. 10 of Jun et al. ('948) clearly shows the stacked diode structure as claimed.

On pps. 6 and 7, applicant attempts to discredit the Jun patent by arguing that the circuit diagram of Fig. 10 cannot be derived from the semiconductor side view shown in Fig. 9.

MPEP 716.07 explains that since in a patent it is presumed that a process if used by one skilled in the art will produce the product or result described therein, such presumption is not overcome by a mere showing that it is possible to operate within the

disclosure without obtaining the alleged product. *In re Weber*, 405 F.2d 1403, 160 USPQ 549 (CCPA 1969).

Therefore, when Jun et al. discloses that Fig. 10 is an accurate circuit diagram of what Fig. 9 purports to be, that presumption is not overcome by applicant's showing that it is possible to obtain a different product than shown.

Also, drawings and pictures can anticipate claims if they clearly show the structure which is claimed. *In re Mraz*, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972). The origin of the drawing is immaterial. For instance, drawings in a design patent can anticipate or make obvious the claimed invention, as can drawings in utility patents. When the reference is a utility patent, it does not matter that the feature shown is unintended or unexplained in the specification. The drawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art. MPEP 2125. *In re Aslanian*, 590 F.2d 911, 200 USPQ 500 (CCPA 1979).

In this case, Fig. 10 of Jun anticipates the claims because the claimed stacked diode structure is clearly shown between the input line and the power lines (Vdd and Vss). As the caselaw indicates, it does not matter that the drawing shown in Fig. 10 is not specifically described in detail, diode by diode, connection by connection, in order to anticipate or make obvious the claimed invention. When Fig. 10 is evaluated for what it reasonably discloses to one of ordinary skill in the art, one would interpret the diagram to be two sets of diode pairs, arranged both in series and in parallel, positioned between an input circuit and an internal circuit; configured for the purpose of ESD protection.

Lastly, on pp. 5, applicant asserts that patentee's disclosure of "large area diodes" as described in column 3, lines 47 and 48 and line 53 does not anticipate the claimed "stacked diodes" of the pending claims. However, applicant overlooks column 3, lines 54 and 55 which give adequate description of patentee's invention:

"Large area diodes provide robust ESD protection. Higher voltages can be withstood by such a design. These large area diodes may be 2 μm by 2 μm up to hundreds of μm in area."

This description, coupled with the Fig. 10 drawing provides further corroboration of the adequacy of the cited prior art. Specifically, Jun et al. discloses that the "large area diodes" are being used for "higher voltages." As is commonly known in the art, silicon diodes normally have a voltage drop of 0.7 volts. By connecting two diodes in series, the voltage drop is increased to 1.4 volts, etc. Since Jun et al. describes using the disclosed device for "high voltages," one of ordinary skill would be able to understand that the depiction of two diodes in series (back-to-back) would be an adequate method of achieving that goal of robust ESD protection.

Second, the term "large area diodes" is adequately described in the disclosure of Jun et al, contrary to applicant's assertion. As quoted above, Jun et al. describes a diode array of "2 μm by 2 μm up to hundreds of μm in area." "Large area" in this sense, clearly also means that a large current is meant to be passed through the diode array. Because, diodes connected in parallel, as opposed to in series, will increase the amount of current that can pass through the diode array.

For these reasons, the rejection of claim 1 over Jun et al. is maintained and examiner seeks affirmation of the Final Rejection.

Rejection of claims 13-17 as being anticipated by Jun et al.

Applicant asserts that the rejection of claim 13 is in error because element 14 is not a source or a drain of the MOS and the examiner has misapplied the reference.

On the contrary, examiner has interpreted the claim terms broadly, and as such, the Jun et al. reference anticipates claim 13. Specifically, applicant claims the semiconductor device of claim 1, "wherein the diode includes a PN junction diode formed by a PN junction between a first source/drain and a substrate of a MOS." As interpreted by the examiner, the PN junction diodes (e.g., Fig. 9) exist at the boundaries between, for example, doped regions 12, 14, 16, and the substrate. The source/drain regions are depicted in Fig. 9 as the regions (32). The substrate is the region (10). Therefore, as claimed, the PN junction regions lay between the source/drain regions and the substrate. Examiner may have inadvertently labeled the region (14) as the source/drain region in Final Rejection. However, this does not excuse the applicant from a correct interpretation of the prior art, nor does it provide a basis to distinguish over the prior art, since the prior art clearly anticipates the claim as written.

Rejection of claims 2-4 as being obvious over Jun et al.

Applicants submit that it would not be obvious to insert a doped area in the first well since there is no indication of doing so and no motivation for providing such a region.

Examiner points applicant's attention to the motivation given in the Final Rejection. Examiner draws on the knowledge known to one of ordinary skill in the art at the time of the invention, coupled with the disclosure of the prior art. Jun et al. discloses providing wells within wells to produce diode structures with high voltages (column 3, lines 53-55). Based on this disclosure, one of ordinary skill in the art at the time of the invention would have been able to insert a third or fourth well into this structure, as stated in the Final Rejection, to increase the threshold voltage of the diode array, thus increasing the voltage drop across the large area diode, as is suggested by the relied upon prior art.

Rejection of claims 5-12 as being obvious over Jun in view of Watt

Regarding claims 5 and 11, applicant argues that the references do not disclose the clamp circuit as claimed. Specifically, applicant argues that the clamps (24 and 26) of Watt are not set between a first and second power line. On the contrary, said clamps (24 and 26, Fig. 5) are clearly placed between two sets of power lines (Vdd1 and Vdd0) and (Vss1 and Vss0). These lines are clearly identified as power lines in the Abstract of Watt and other places throughout the disclosure. Therefore, the prior art reads on the claims.

In re claims 12 and 15, applicant concedes that the prior art reference discloses the MOS diode as claimed, but argues that examiner does not provide motivation in coupling the gate to the source/drain region. Examiner asserts that the previously provided motivation is sufficient. Watt discloses using the claimed structure as a secondary ESD protection circuit. Connecting the gate region to the source/drain is a configuration well known in the art. For example, applicant is directed to a general prior art device, Assaderaghi et al. (U.S. Patent No. 5,811,857), which discloses in its Abstract that connecting the gate to the drain region is just a way to provide ESD protection. Such an explanation is analogous to that provided by the examiner in the final rejection.

In re claim 6, applicant asserts that claim 6 is allowable because the source and drain regions are not connected to Vss1 and Vdd1, instead they are connected to Vss0 and Vdd0. Examiner disagrees. In the body of the rejection, examiner refers to output buffer circuit (14) which contains source/drain regions (34 and 36). However, the claim circuit also contains the input buffer circuit (12) which has source/drain regions directly connected to Vss1 and Vdd1. If the prior art cited by the examiner anticipates or makes obvious the claimed invention, but does not spell out every detail, applicant is still held to the teachings disclosed therein.

Regarding claims 7 and 8, applicant asserts that the gate electrode regions are not shown to be applied with a bias voltage. Examiner asserts that biasing the gate of a transistor device is well known to those of ordinary skill in the art. Doing so is not just common, it is very much required in most cases to provide the necessary conduction

current to pass electrons or holes across the MOS channel region. In most instances, the transistor device would not function without this most basic reference bias. Therefore, if the prior art does not disclose the gate biases specifically, this is because such a configuration is so obvious in the art as to not deem a separate teaching.

Regarding claims 9 and 10, applicant claims isolation wells and argues that such are not disclosed in the prior art. Again, isolation wells in this technology are components of basic design structure. As stated in the rejection, it is very often the practice in semiconductor design to place operable wells within sub-surface wells to protect upper circuits from underlying current and voltage drops. Such features are well known in the art and the claiming of such does not demonstrate novel subject matter in this case.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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SUPERVISORY PATENT EXAMINER

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